

Figure 1a

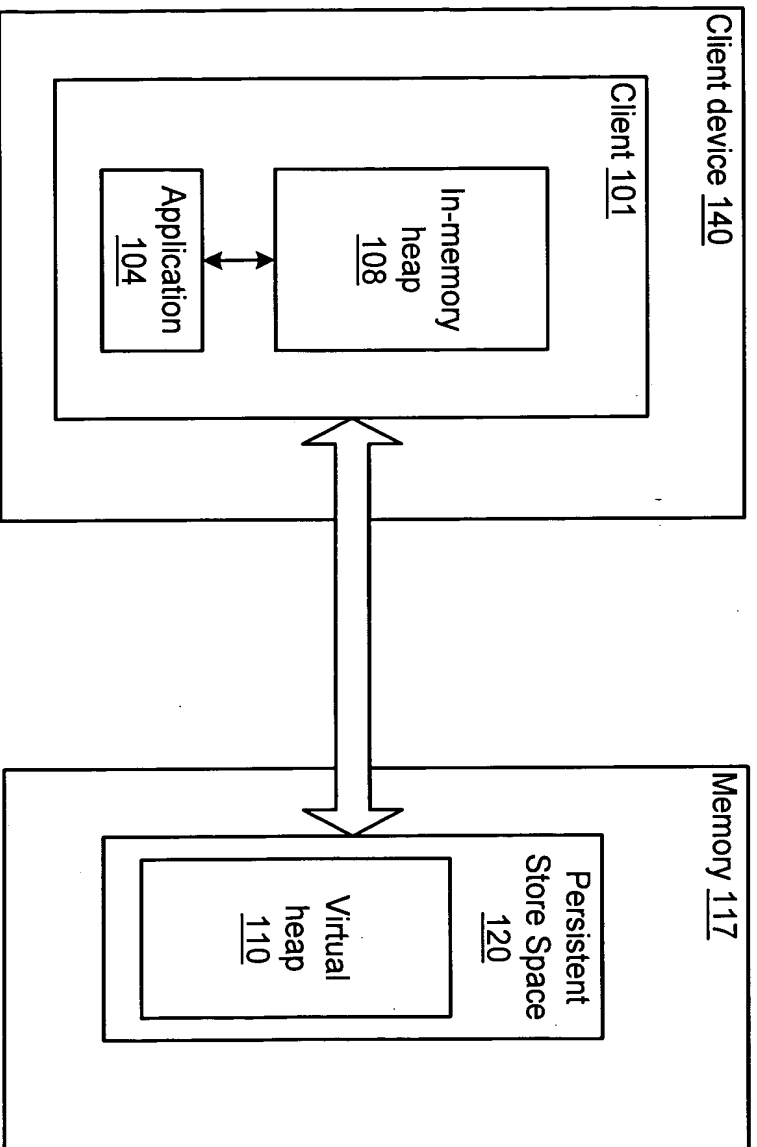


Figure 1b

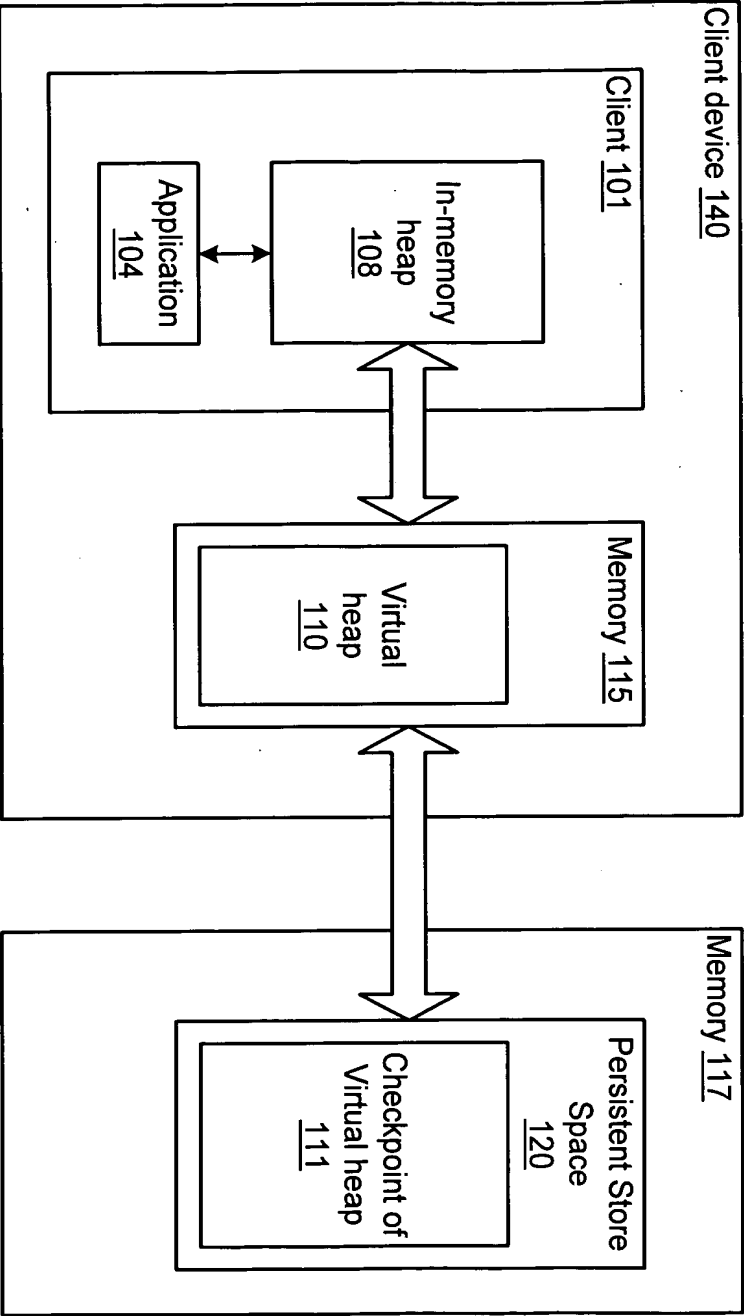


Figure 1c

FIG. 1c is a block diagram of a client device 140 and a memory system 115, 117, according to one embodiment.

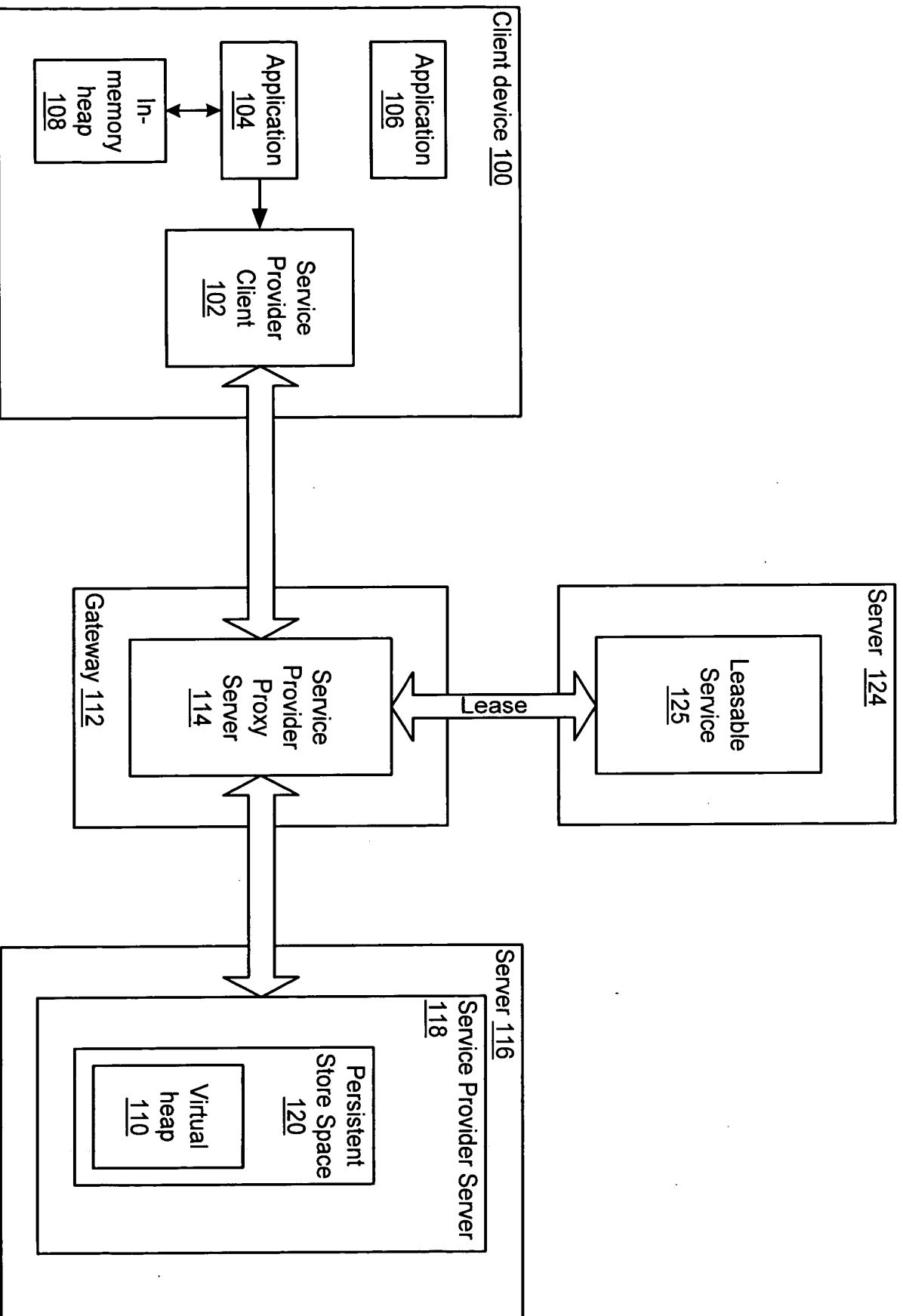


Figure 1d

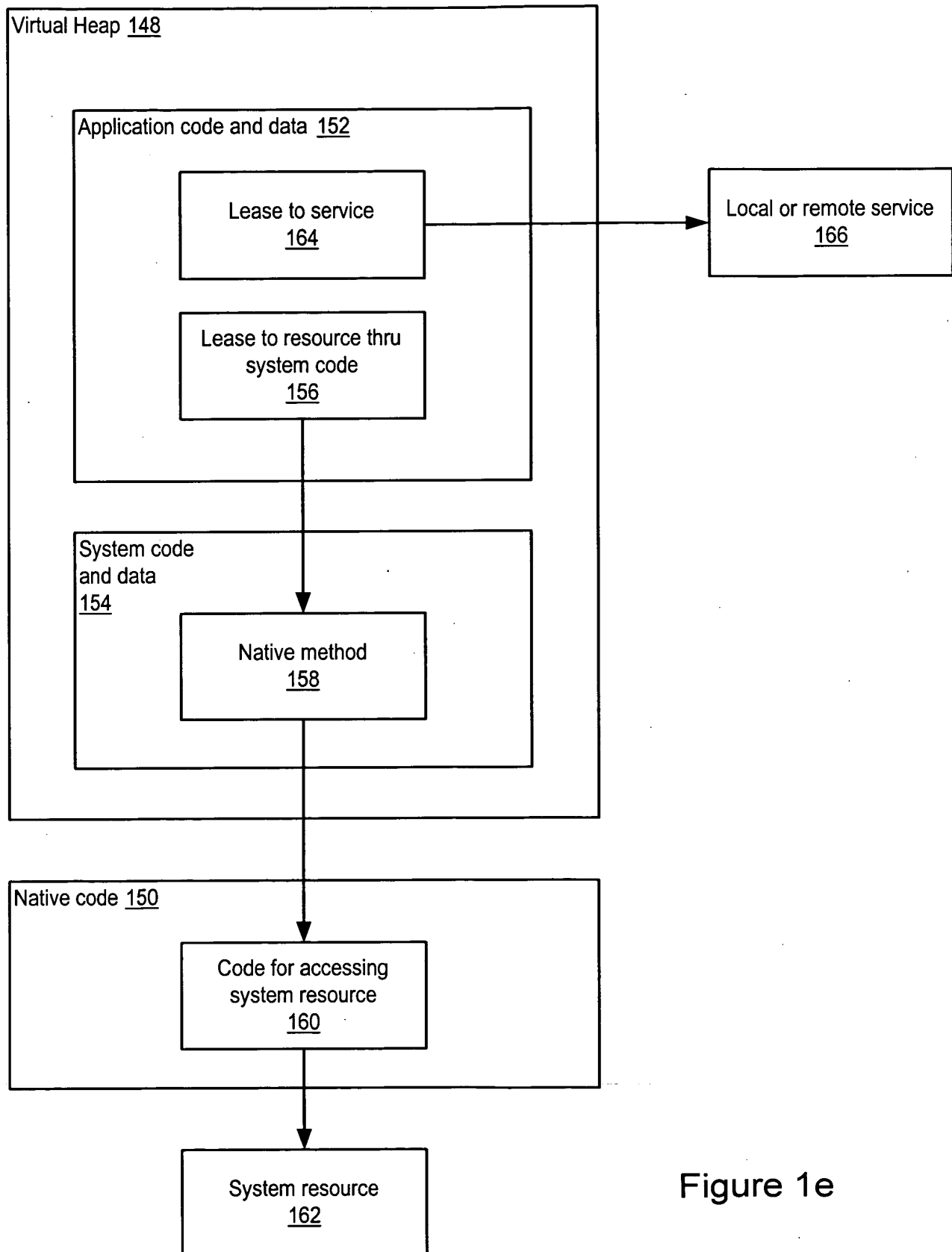


Figure 1e

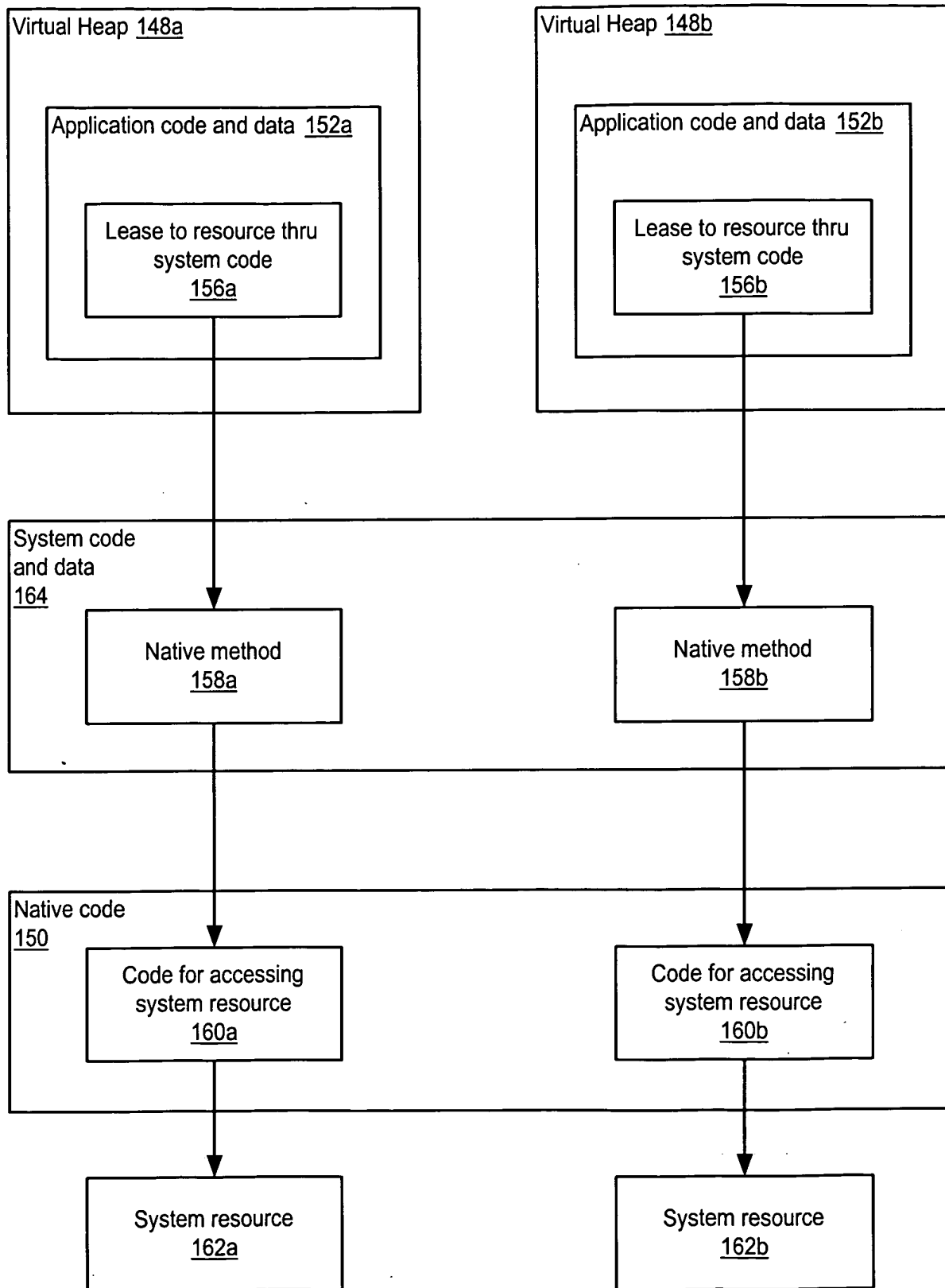
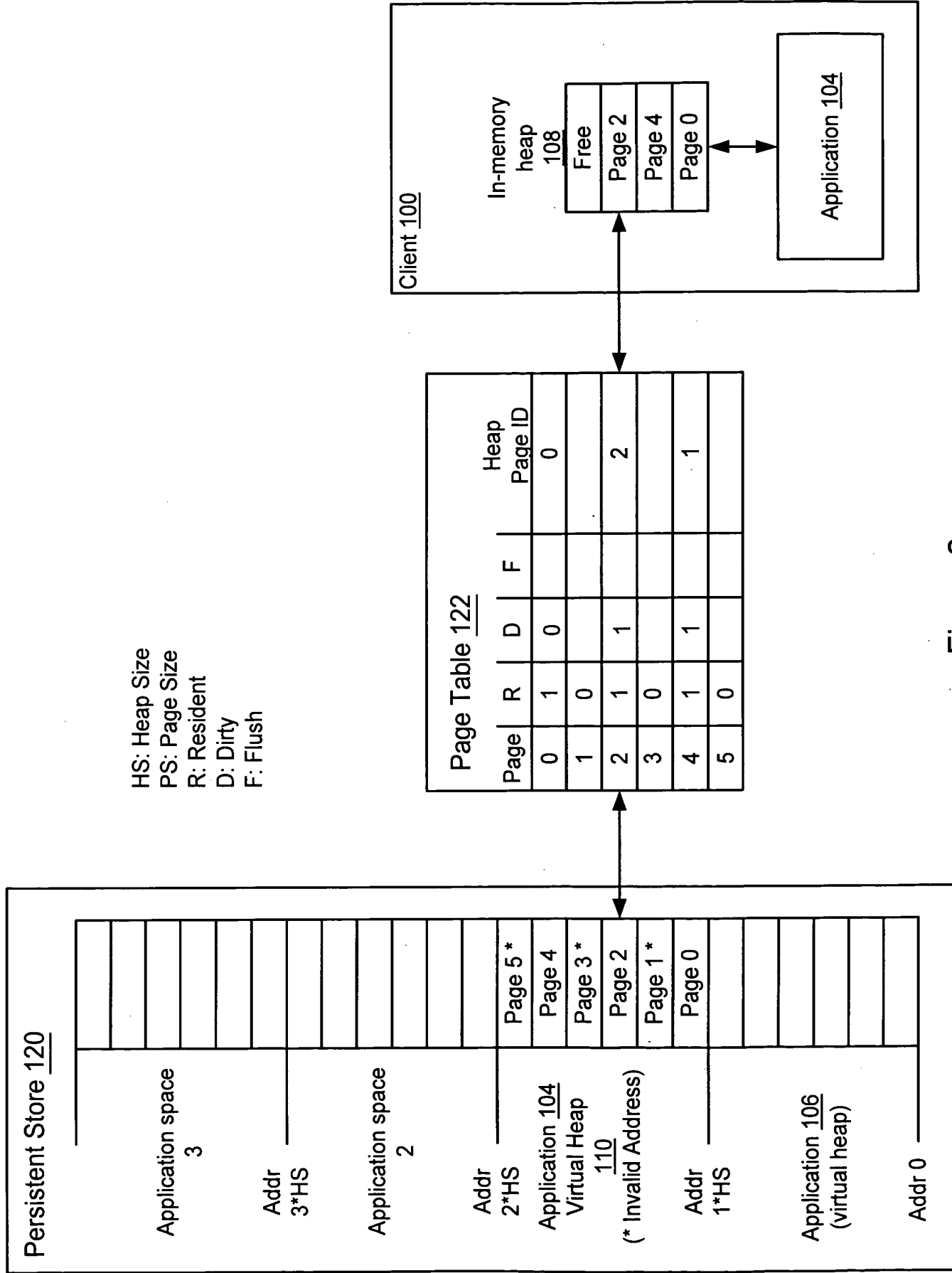


Figure 1f

Figure 2 illustrates the mapping of application memory to persistent storage. The diagram shows the flow of data from the application's in-memory heap to the persistent store via a page table.



HS: Heap Size  
PS: Page Size  
R: Resident  
D: Dirty  
F: Flush

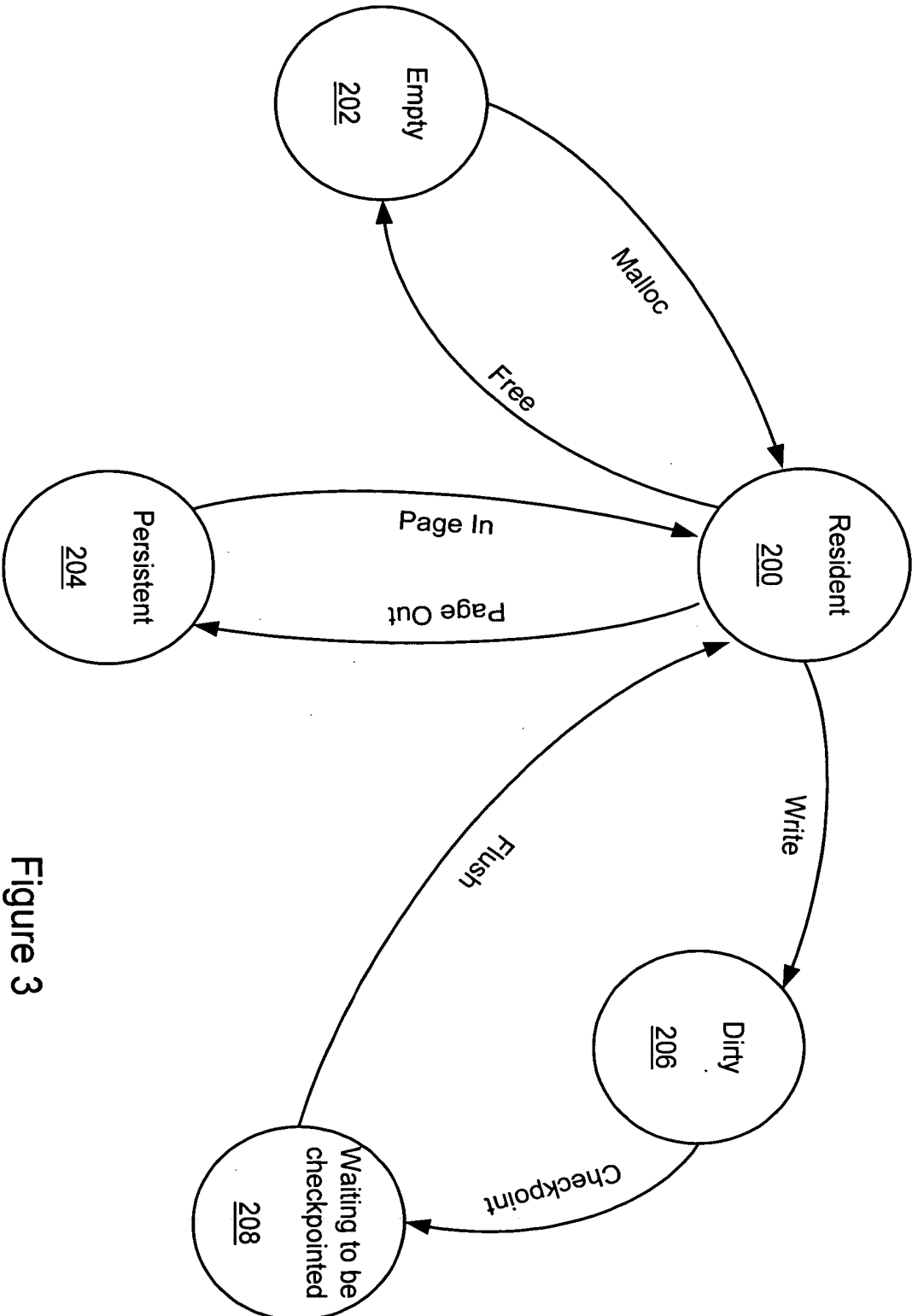


Figure 3



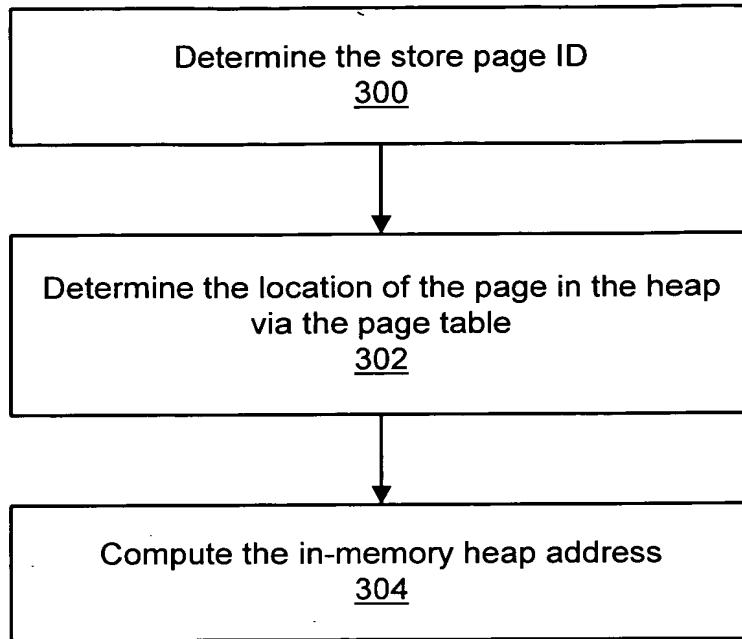


Figure 4

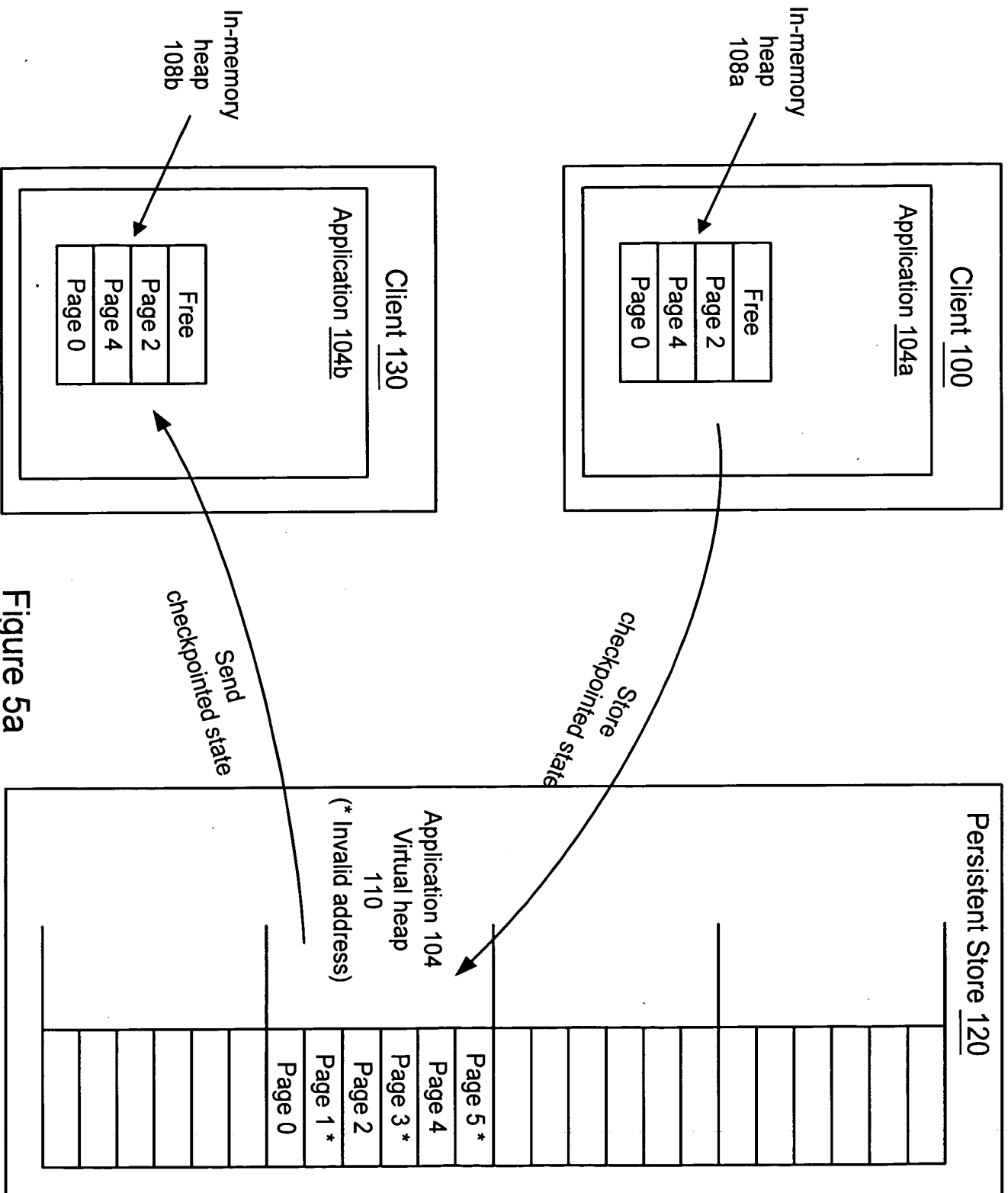


Figure 5a

FIG. 5a is a block diagram of a system architecture for memory checkpointing.

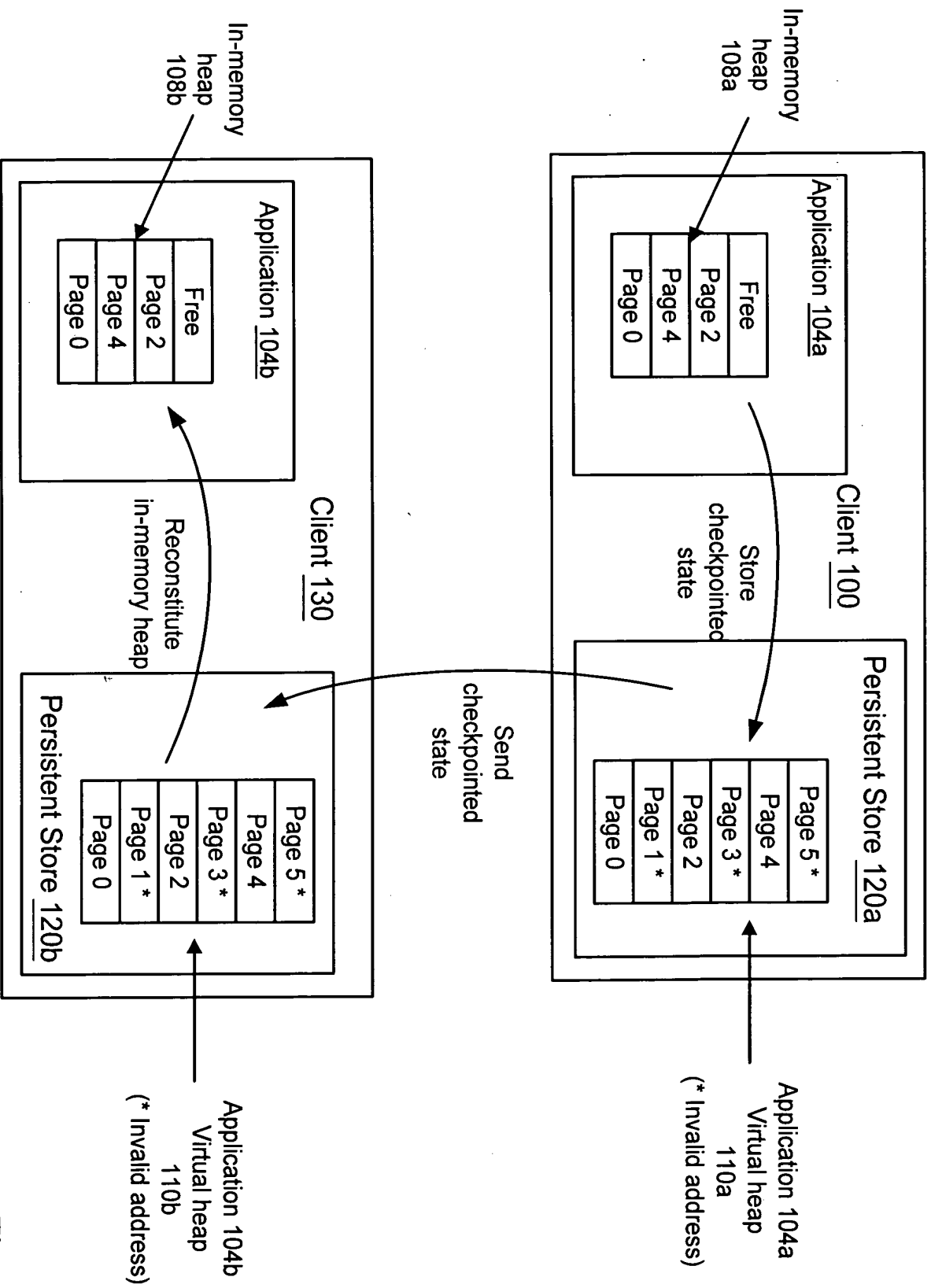


Figure 5b

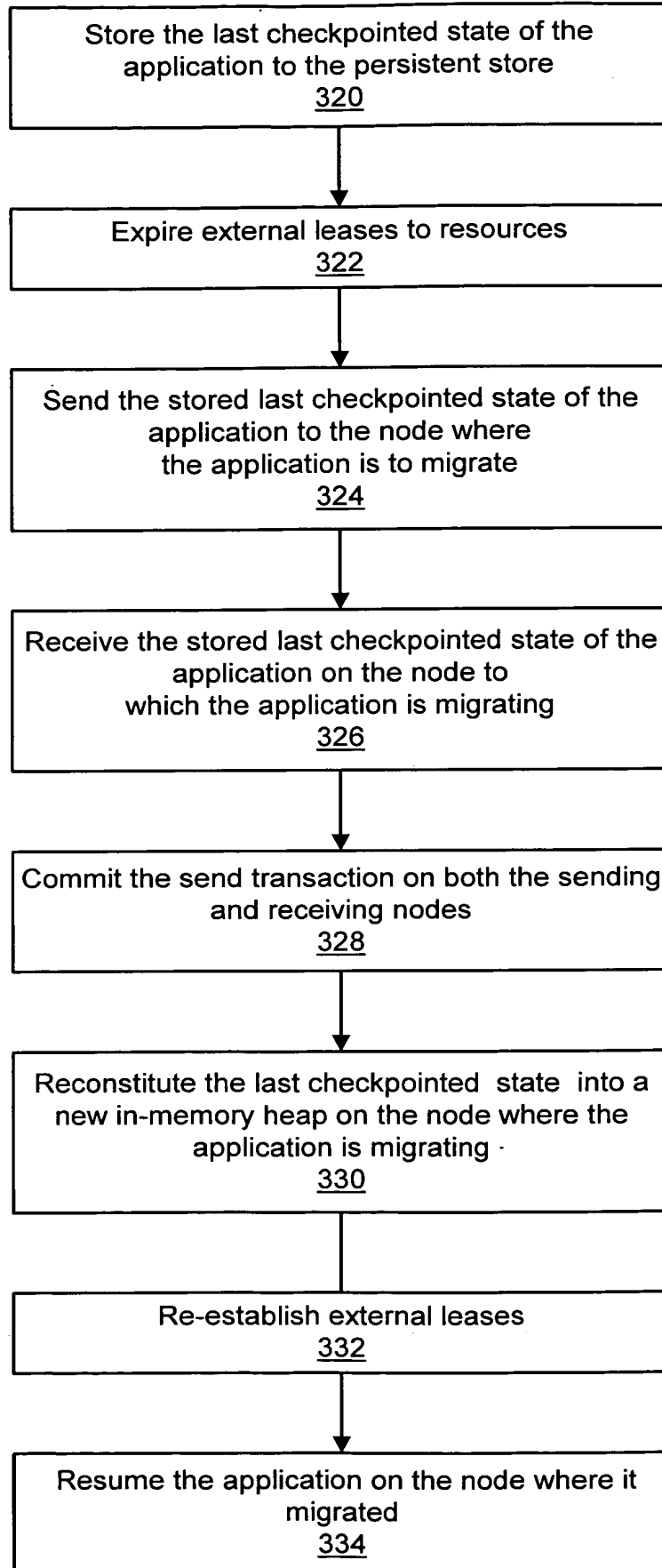
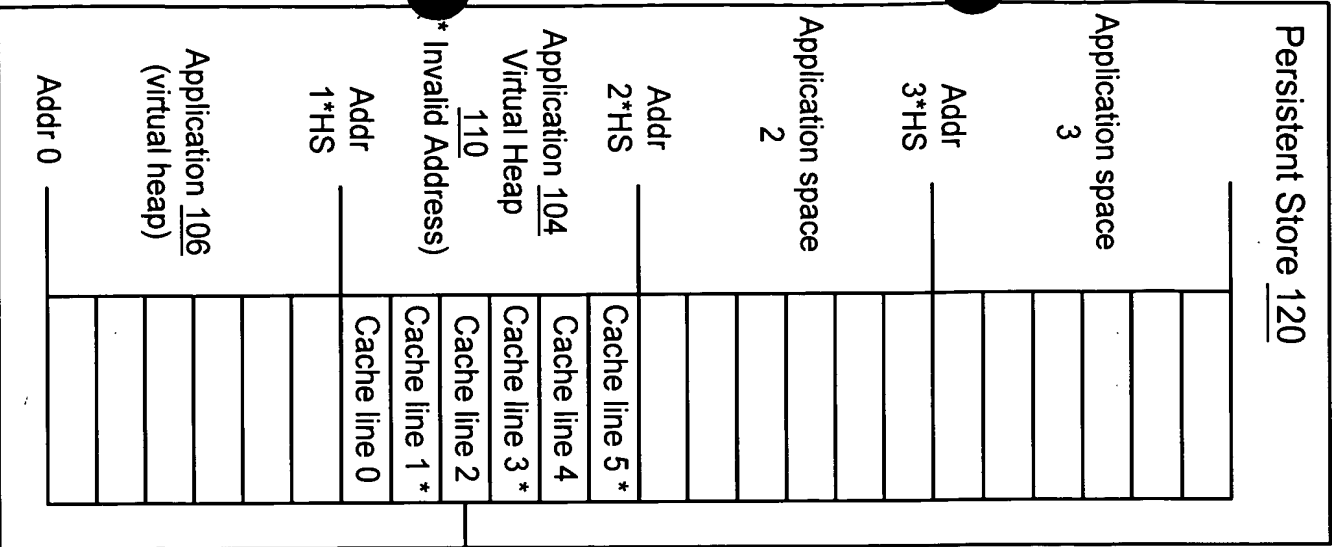


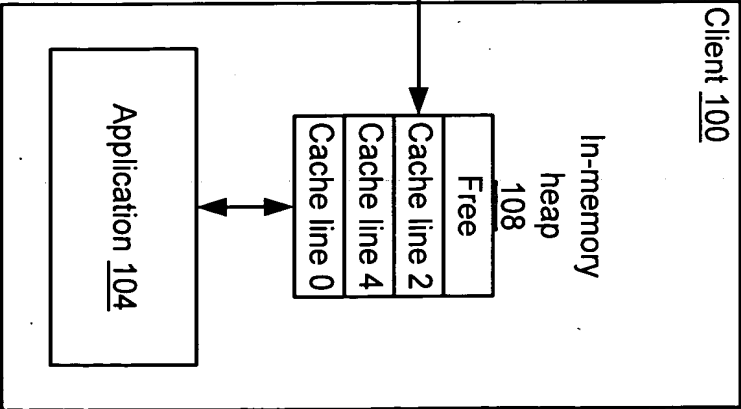
Figure 6



HS: Heap Size  
CS: Cache Line Size  
R: Resident  
D: Dirty  
F: Flush

Cache Table <u>122</u>					Heap Cache line ID	
Page	R	D	F			
0	1	0			0	
1	0					
2	1	1			2	
3	0					
4	1	1				1
5	0					

Figure 7



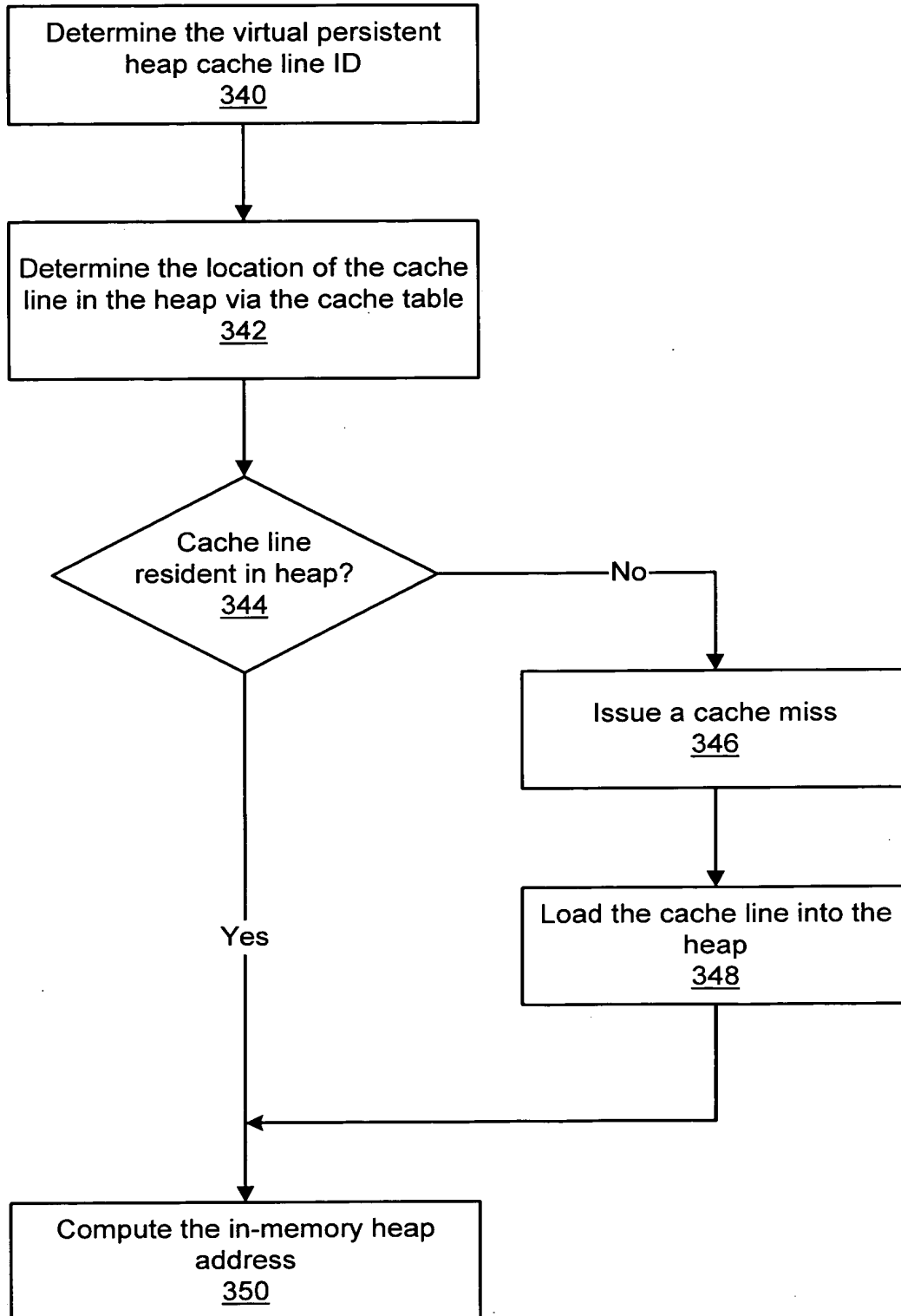


Figure 8

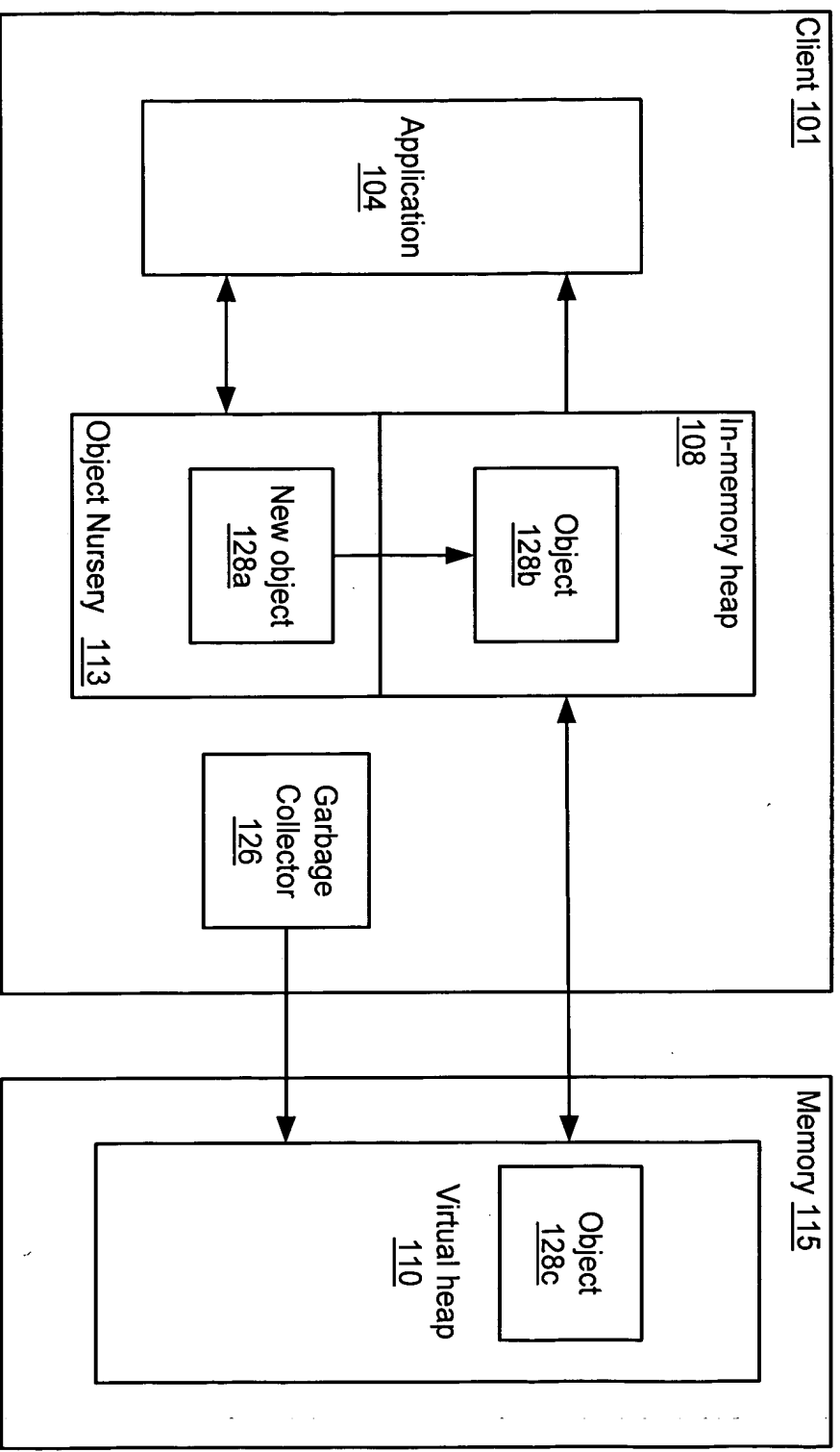


Figure 9

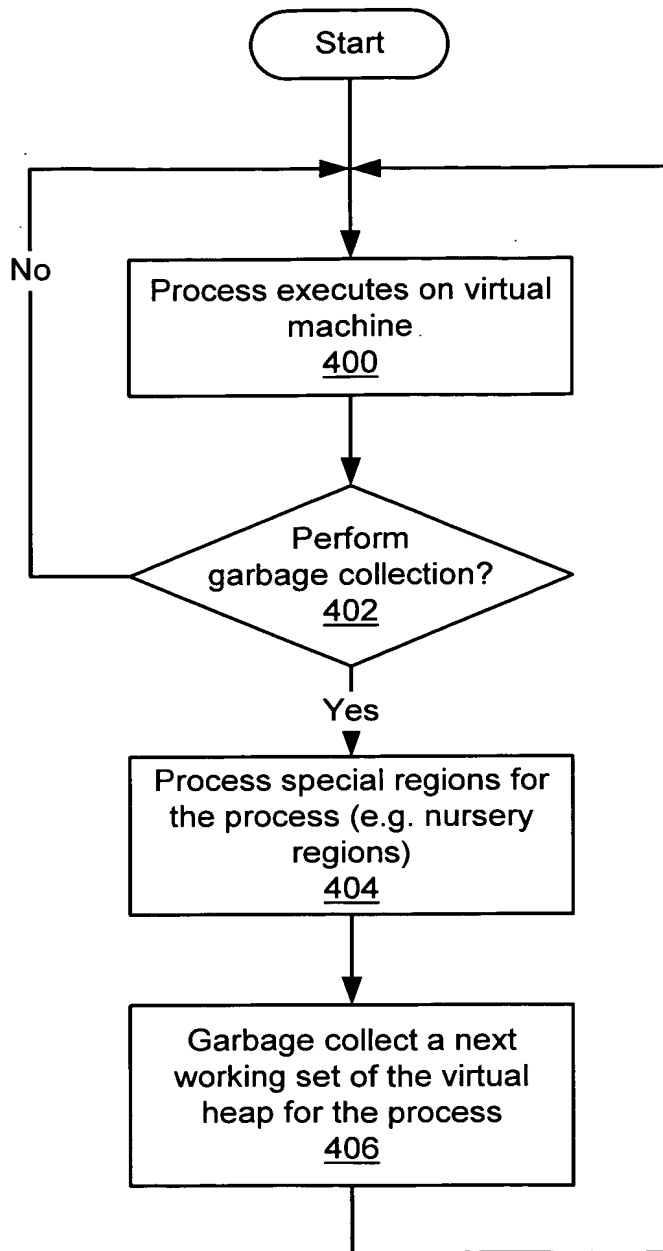


Figure 10a



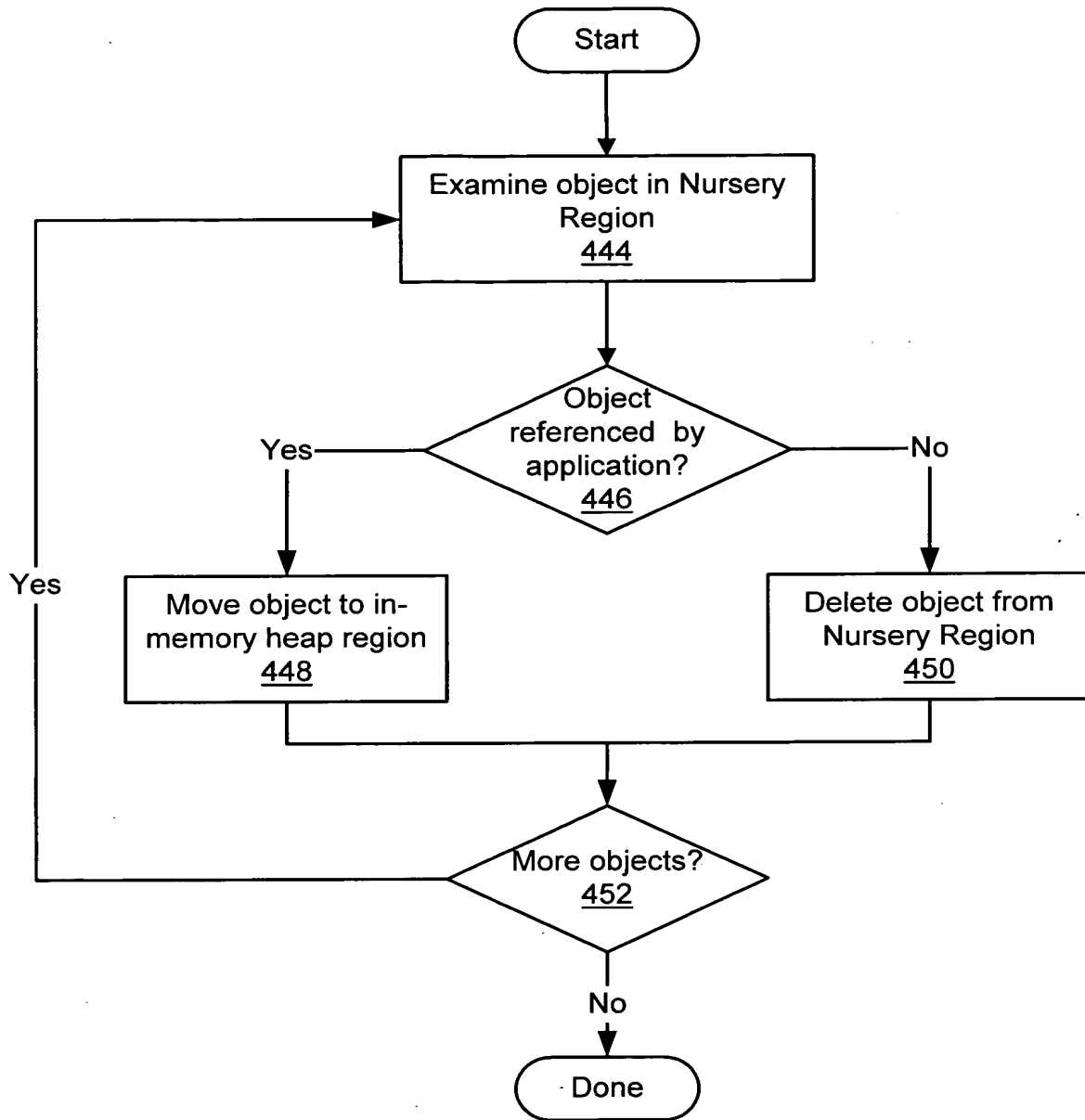


Figure 10b

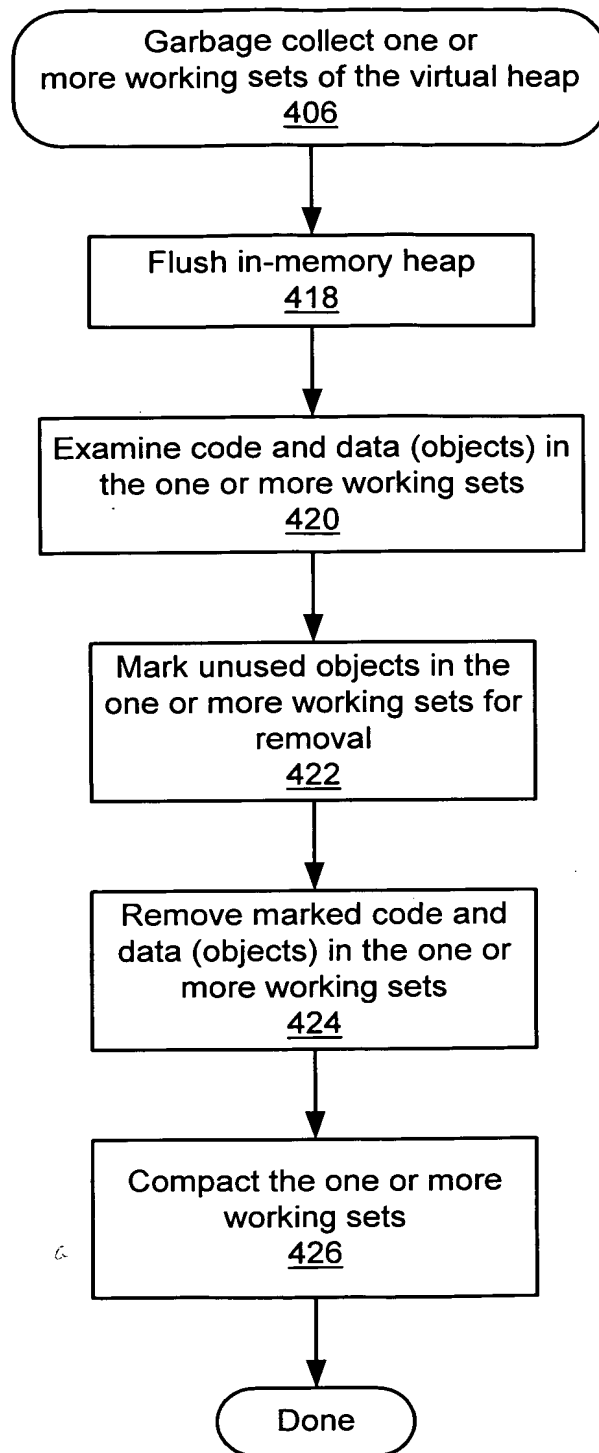


Figure 10c

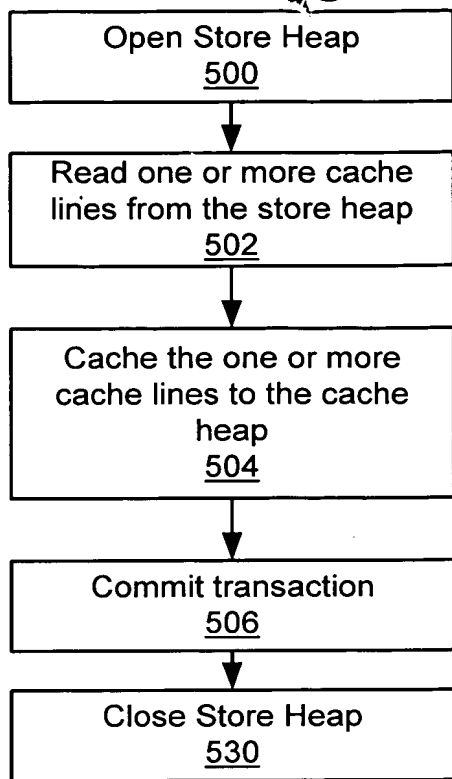


Figure 11a

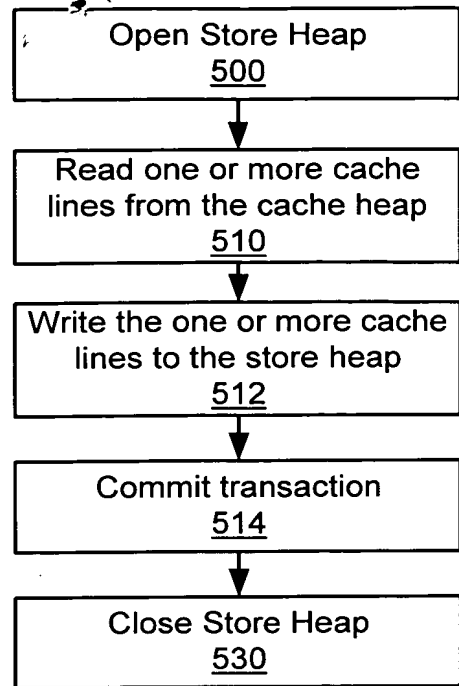


Figure 11b

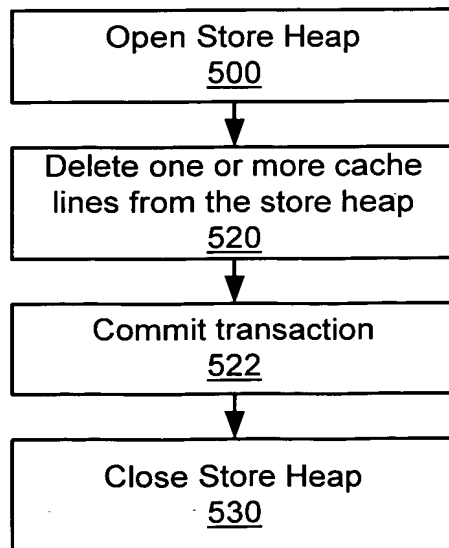


Figure 11c